REMARKS

Claims 6 and 9-16 are pending. Claims 1-5 and 7-8 were cancelled in the previous amendment without prejudice. Claims 6, 9, 12, and 13 have been amended. No new matter has been added. The specification supports first and second multiplexers selecting a data set from a plurality of data sets at least on page 3, line 19 - page 4, line 18 and page 6, line 16 - page 7, line 2. Reconsideration and allowance of the presently amended application are respectfully requested.

Claim Rejections Under Double Patenting:

Claims 1-16 stand rejected under the judicially created doctrine of obviousness-type double patenting as allegedly being unpatentable over claims 1-10 of U.S. Patent No. 6,725,360 to Aldrich et al. ("Aldrich"). Applicant respectfully traverses the double patenting rejections. The present application is a divisional of Applicant's prior Application No. 09/541,116 (now U.S. Patent No. 6,725,360), the same reference relied upon by the Office Action to allege the double patent rejections. The present application is directed to the non-elected claims resulting from the restriction requirement applied by the Office in the parent application, Aldrich, and thus the present

application cannot be held as being the same invention as the parent application. MPEP § 806.05 adds that "[i]f nondistinct inventions are claimed in separate applications or patents, double patenting must be held, ***except where the additional applications were filed consonant with a requirement to restrict in a national application.***" (Emphasis added).

Further, MPEP § 804.01 clearly prohibits certain kinds of double patenting rejections under 35 U.S.C. § 121.

> 35 U.S.C. § 121 authorizes the Commissioner to restrict the claims in a patent application to a single invention when independent and distinct inventions are presented for examination. ***The third sentence of 35 U.S.C. § 121 prohibits the use of a patent issuing on an application with respect to which a requirement for restriction has been made, or on an application filed as a result of such a requirement, as a reference against any divisional application, if the divisional application is filed before the issuance of the patent. The 35 U.S.C. § 121 prohibition applies only where the Office has made a requirement for restriction***. The prohibition does not apply where the divisional application was voluntarily filed by the applicant and not in response to an Office requirement for restriction. This apparent nullification of double patenting as a ground of rejection or invalidity in such cases imposes a heavy burden on the Office to guard against erroneous requirements for restrictions where the claims define essentially the same invention in different language and which, if acquiesced in, might result in the issuance of several patents for the same invention. (Emphasis added).

Applicant submits that claims 1-16 of the present application are distinctly patentable over the parent

application. For at least these reasons, claims 1-16 are not properly rejected based on double patenting over Aldrich.

Claim Rejections Under 35 U.S.C. § 102 (e)

Claims 6 and 9-16 stand rejected as allegedly being anticipated by U.S. Patent No. 6,092,094 to Ireton ("Ireton"). These contentions are respectfully traversed.

Claim 6

Ireton fails to teach ***a first multiplexer and a second multiplexer operative to receive a plurality of n-bit data sets from the bus and to select a single n-bit data set from the plurality of n-bit data sets to be processed*** as recited in claim 6. In fact, Ireton does not disclose any multiplexer that receives data sets from the bus and selects a single n-bit data sets as recited in claim 6. In contrast, Ireton teaches sending the operands to an adder and a multiplier directly from first and second operand buses. *See*, Col. 7, lines 10-47 and FIG. 2.

> A first operand corresponding to the decoded instruction is received upon a first operand bus 42, while second operand is received upon a second operand bus 44...Both first operand bus 42 and second operand bus 44 are coupled to both adder circuit 50 and multiplier circuit 54.

Further, Ireton fails to teach *configuring the multiplier into the first structure of a single n-bit multiplier* ***when the***

data is greater than (n/2)-bits *and configuring the multiplier into the second structure of two (n/2)-bit multiplier* ***when the data is (n/2)-bits or less*** as required in claim 6. In Ireton, "[c]ontrol signals asserted in response to the instruction conveyed thereto are used to configure the integer operation circuit for narrow-width or wide-width computations." (Col. 4, lines 40-43; Col. 7, lines 58-63; and FIGS. 2-5). The control signal instructs the multiplication circuit 54 to process the 32 bit data as narrower width operands using individual multiplier circuits 90 as shown in FIG. 5. Therefore, multiplier circuits are not configured in response to determined size of the data rather they are configured based on the control signals from the control unit 46.

For at least these reasons, claim 6 is allowable over Ireton.

Claims 9-11

Claims 9-11 are dependent upon claim 6 and thus are patentable over Ireton for at least the reasons set forth with respect to claim 6 above.

In addition, Ireton fails to teach ***a plurality of arithmetic logic units to collect the processed data set through a plurality of multiplexers*** as recited in claim 9. In contrast, Ireton teaches collecting the results from the adder circuit 50

and the multiplier circuit 54 using the multiplexer circuit 56 without teaching or suggesting a plurality of arithmetic logic and a plurality of multiplexers as recited in claim 9 (col. 7, lines 25-27 and FIG. 2). A multiplexer is not an arithmetic logic unit (ALU) since it does not perform arithmetic or logic operation as required for an ALU. Therefore Ireton fails to teach a plurality of multiplexers that selects the processed data and a plurality of arithmetic logic units that collects the processed data after they pass through the plurality of multiplexers.

Ireton also fails to teach ***a flop which stores the result of the multiplier*** as recited in claim 10 and ***at least one arithmetic logic unit which adds the result from the multiplier to a running total*** as recited in claim 11. In Ireton, the control unit 46 sends a selection line 58 to the multiplexer circuit 56 holding the results, whereby a result is selected and transmitted to a result bus 26 (col. 7, lines 25-31 and FIG. 2). Ireton does not disclose ***a flop*** for storing the results or a arithmetic logic unit for adding to a running total as recited in claims 9-11.

For at least these additional reasons, claims 9-11 are patentable over Ireton.

Claim 12

Claim 12: A method comprising:
selecting a single n-bit data set from a plurality of data sets;
determining a size of the ***selected data set*** to be processed;
configuring a first processing path for data set of n-bits if the ***selected data set*** size is greater than (n/m)-bits; and
dividing the first processing path into multiple processing paths if the ***selected data set*** size is (n/m)-bits or less.

As set forth with respect to claim 1 above, Ireton does not teach selecting a single n-bit data set from a plurality of data sets. For example, there are no multiplexers to select ***a single n-bit data set from a plurality of data sets*** placed upstream of the adder or the multiplier in Ireton. Ireton sends the operands directly to the adder and multiplier. Therefore, Ireton does not teach configuring the first processing based on the size of the ***selected data set***.

In addition, Ireton teaches using execution units 20 to execute instructions specifying wide operands and single instruction multiple data (SIMD) instructions specifying multiple narrow operands. (col. 4, lines 8-11). Integer operation circuits of the execution units 20 are ***configured to interpret the operands either as single values of particular***

width or as multiple independent values of narrower widths depending on the instructions (col. 4, lines 11-17). Thus, Ireton does not configure or divide the first processing path based on the size of the ***selected data set*** as recited in claim 1. Rather, Ireton's execute instructions specify how the operand should be ***interpreted*** and processed.

> *For example, if the integer operation circuits are configured to operate upon 32 bit operands and the particular SIMD instruction specifies 4 bit operands, then eight independent values from each operand are operated upon and eight independent results are produced.* (col. 4, lines 25-29).

Thus, Ireton relies on the execution instructions to specify how the operands should be operated and does not configure or divide the first processing path if the ***selected*** data set is greater than or equal to/less than (n/m)-bits.

For at least this reason, claim 12 is patentable over Ireton.

Claims 13-16

Claims 13-16 depend from claim 12 and thus are patentable over Ireton for at least reasons stated for claim 12 above.

CONCLUSION

It is believed that all of the pending claims have been addressed in this paper. However, failure to address a specific rejection, issue, or comment, does not signify agreement with or

concession of that rejection, issue or comment. In addition, because the arguments made above are not intended to be exhaustive, there may be reasons for patentability of any or all pending claims (or other claims) that have not been expressed. Finally, nothing in this paper should be construed as an intent to concede any issue with regard to any claim, except as specifically stated in this paper, and the amendment of any claim does not necessarily signify concession of unpatentability of the claim prior to its amendment.

Claims 1-2, 4-6, and 9-16 are in condition for allowance, and a notice to that effect is respectfully solicited.

Please apply the total amount of $2,380 ($790 for Request for Continued Examination; and $1,590 for Extension of Time fee), and apply any additional fees or any credits to deposit account 06-1050, referencing the attorney docket number shown above.

Respectfully submitted,

Date: December 2, 2005

Scott C. Harris
Reg. No. 32,030

Fish & Richardson P.C.
12390 El Camino Real
San Diego, California 92130
Telephone: (858) 678-5070
Facsimile: (858) 678-5099
10573166.doc